University of Dayton

ECE

Mumma Radar Lab

Comprehensive VHDL

Fall 2016

Final Exam

Due on 12/12/2016

***Part A***

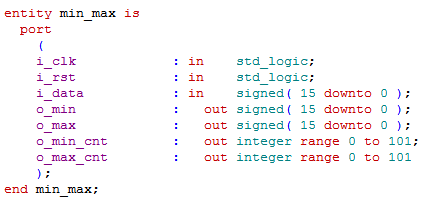
25%

*Simulation only.*

Design a VHDL block that can find and count the minimum and the maximum values of the incoming data (data.txt)

Your test bench should print out on the message window the number of min and max values as well as how many of these value in the incoming data.

Please use the following entity:



***Part B***

75%

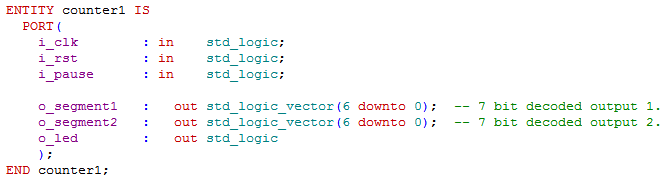
*Simulation and FPGA*.

Design a counter that counts from 0 to 99. It should increment each `1 second.

Show the counter outputs on the 7 segment displays on the FPGA board.

Please add pause signal to stop the counter as needed. Also add LED signal to show that the code got configured fine.

Please use the following entity:



Please submits all you VHDL codes, TCL files. And your reports.

Make sure to show your counter’s result on the FPGA board to your TA on the due date.